Automatically Disconnecting ICSP PIC Programmer

"APIC Programmer"

Aruna P. Rubasinghe
University of Moratuwa (ENTC), Sri Lanka
9/5/2009

2

Index:

"APIC Programmer"

Introduction

JDM programmers are the most using homemade programmers. There are several draw backs in cheap JDM based ICSP programmers. We can list them as follows

1. JDM based ICSP programmers require, user to disconnect ICSP cable from target board before executing program. Otherwise target board will not operate properly. This because programmer begins to act as external component to target board and most importantly negative voltage on MCLR pin will reset the PIC.

2. User has to remove the power supply to target board before begin programming. Not removing external power supply normally causes erroneous programming. This is because JDM programmers use funky voltages. Separate power supply will interfere with programmer.

3. These JDM programmers depend on the charge stored in a capacitor to supply Vpp voltage during programming. Programming errors may occur when writing large programmers where charge on capacitor drains before completing programming.

4. Removing ICSP cable after programming may damage PIC because these programmers continuously provide 5V even after programming is complete.

5. Most JDM programmers do not give user to select method to enter programming modes "Vpp before Vdd" or "Vdd before Vpp". (There are few improved programmers which has this option)

Features

In order to solve above problems I designed this PIC programmer. Following are the features of this programmer.

Programmer will automatically disconnect from target board after programming is complete.

❖ User does not have to remove ICSP cable manually. Programmer will automatically connect to target board when programming begins. This is achieved by using CD4066 bilateral switch. This IC contains 4 bilateral switches. These switches turns on when their control pins states are high and goes to high impedance mode when control pins states are low. These high impedance state acts as disconnection of programmer's Vpp, Vdd, clock and data lines are connected to target board through these switches. Normally all switch control pins are set to logic low by using pull down resistor. Therefore programmer is disconnected from target board. When programming begins, TXD pin of serial port goes high (positive 12V) and this will set control pins logic state to high and this will turn on switches. So programmer will connects to target board through switches and programming begins.CD4066 has maximum

supply voltages of 15V therefore it can be connected to TXD pin directly. Since programmer is disconnected and MCLR pin is set to high so program execution can begin immediately.

No need to remove external power supply to target board even programmer is self powered.

❖ This programmer use rectifying bridge to convert negative voltage (-12V) at TXD pin respective to GND pin of serial port, when not in programming mode. And when in programming mode TXD voltage with respective to GND pin becomes positive. Due to rectifying bridge output is always positive. This positive output voltage is regulated and reduced to 5V supply using a 78L05 regulator IC. Therefore external power supply to PIC and programmers power supply matches. Therefore we don't have to remove the external power supply.

Programmer does not depend on charge stored in a capacitor to supply Vpp voltage

❖ Programmers Vpp supply is taken through the rectifier bridge. In order to reduce voltage drop on bridge germanium diodes (OA70) are used. Normally serial port can supply 12V and most PICs have programming voltage between 8.5V-13.5V this is enough without charge pump capacitor. So we can write large programs without failing.
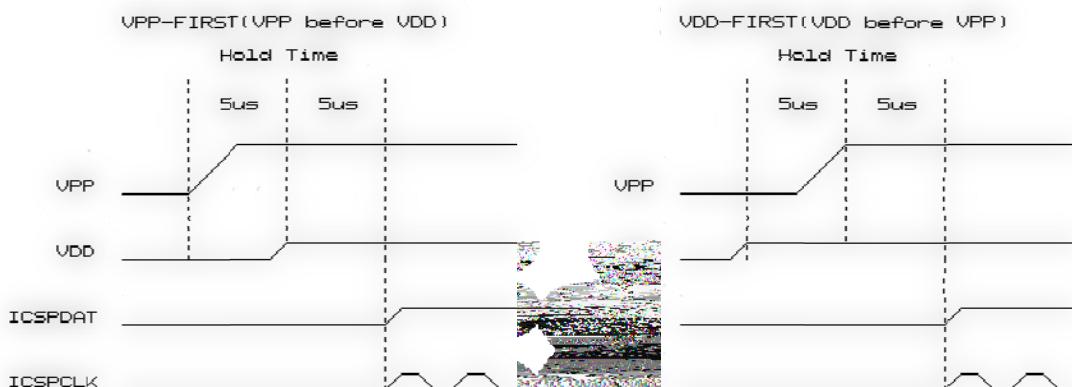
Removing ICSP cable does not damage PIC

❖ This is because programmer disconnects itself from target board and power supply with it. Removing cable will not do anything.

"Vpp before Vdd", "Vdd before Vpp" and "Vpp during Vdd" method selection ability

❖ Some PICs requires Vpp before Vdd method to program (12F675) and some requires Vdd before Vpp method (18F452, 16F876). This is achieved by simple RC delay circuit. When Switch S1 is on position 1, Vpp is directly supplied to PIC but Vdd is delayed by charging capacitor C4 through R4.when Switch is set to position 3 Vdd is directly supplied without

Two methods that enter devices into Program/Verify mode

5

delay but Vpp supply is delayed until capacitor C5 charge through R5 to required voltage. By setting switch to center position (2) "Vpp during Vdd" is selected.

Cheap

❖ It cost only about <u>$ 0.77</u>
   ✓ CD4066 – $ 0.25
   ✓ 78L05 - $ 0.10
   ✓ Resistors - $ 0.03
   ✓ Capacitors - $ 0.06
   ✓ Diodes - $ 0.08
   ✓ Switch - $ 0.25

"APIC Programmer"

Schematic

VPP

VDD

DAT

CLK

C5
0.01uF

Vdd before Vpp

GND

D1
OA70 x 4

TXD (3)

GND (5)

RTS (7)

DTR (4)

CTS (8)

Programming voltages and methods

```
;****************************************************************
;
; 18F Device Table
;
;   <ID2> <ID1> <"name"> <param1> <param2>, 8 bytes per device
;
; PARAM1 = B EE WWWW F  (B = bulk erase algorithm, 0 or 1)
;                       (E = erase buffer size, 20h or 40h)
;                       (W = write buffer size, 08h, 20h, or 40h)
;                       (F = flash memory size b16)
;
; PARAM2 = FFFF EEEE    (F = flash mem size b15..b12)
;                       (E = eeprom mem size b11..b8)
;
```

<div style="text-align:right">Programming Voltage   Programming method</div>

```
        org    h'0C00'

ID8TBL  dt   0x04,0x80, "242 ", 0x42,0x41    ;18F242    9.0-13.25 VDD
        dt      0x08,0x00, "248 ", 0x42,0x41  ;18F248    9.0-13.25 VDD
        dt      0x04,0x00, "252 ", 0x42,0x81  ;18F252    9.0-13.25 VDD
        dt      0x08,0x40, "258 ", 0x42,0x81  ;18F258    9.0-13.25 VDD
        dt      0x04,0xA0, "442 ", 0x42,0x41  ;18F442    9.0-13.25 VDD
        dt      0x08,0x20, "448 ", 0x42,0x41  ;18F448    9.0-13.25 VDD
        dt      0x04,0x20, "452 ", 0x42,0x81  ;18F452    9.0-13.25 VDD
        dt      0x08,0x60, "458 ", 0x42,0x81  ;18F458    9.0-13.25 VDD


        dt      0x07,0xE0, "1220", 0x42,0x11  ;18F1220   9.0-13.25 VDD
        dt      0x05,0x80, "2220", 0x42,0x11  ;18F2220   9.0-13.25 VDD
        dt      0x05,0xA0, "4220", 0x42,0x11  ;18F4220   9.0-13.25 VDD
        dt      0x07,0xC0, "1320", 0x42,0x21  ;18F1320   9.0-13.25 VDD
        dt      0x05,0x00, "2320", 0x42,0x21  ;18F2320   9.0-13.25 VDD
        dt      0x05,0x20, "4320", 0x42,0x21  ;18F4320   9.0-13.25 VDD


        dt      0x08,0xE0, "2331", 0x42,0x21  ;18F2331   9.0-13.25 VDD
        dt      0x08,0xC0, "2431", 0x42,0x41  ;18F2431   9.0-13.25 VDD
        dt      0x08,0xA0, "4331", 0x42,0x21  ;18F4331   9.0-13.25 VDD
        dt      0x08,0x80, "4431", 0x42,0x41  ;18F4431   9.0-13.25 VDD


        dt      0x21,0x60, "2221", 0xC2,0x11  ;18F2221   9.0-12.5  VDD (e)
```

```
        dt      0x21,0x20, "2321", 0xC2,0x11   ;18F2321   9.0-12.5   VDD (e)
        dt      0x11,0x60, "2410", 0xC8,0x40   ;18F2410   9.0-12.5   VDD (e)
        dt      0x11,0x40, "2420", 0xC8,0x41   ;18F2420   9.0-12.5   VDD (e)
        dt      0x24,0x20, "2450", 0xC8,0x40   ;18F2450   9.0-12.5   VDD (f)
check
        dt      0x0B,0xA0, "2455", 0xC8,0x61   ;18F2455   9.0-12.5   VDD
        dt      0x1A,0xE0, "2480", 0xC8,0x41   ;18F2480   9.0-12.5   VDD (e)
        dt      0x11,0x20, "2510", 0xC8,0x80   ;18F2510   9.0-12.5   VDD (e)
        dt      0x0C,0xE0, "2515", 0xD0,0xC0   ;18F2515   9.0-12.5   VDD
        dt      0x11,0x00, "2520", 0xC8,0x81   ;18F2520   9.0-12.5   VDD (e)
        dt      0x0C,0xC0, "2525", 0xD0,0xC4   ;18F2525   9.0-12.5   VDD
        dt      0x0B,0x60, "2550", 0xC8,0x81   ;18F2550   9.0-12.5   VDD
        dt      0x1A,0xC0, "2580", 0xC8,0x81   ;18F2580   9.0-12.5   VDD (e)
        dt      0x0E,0xE0, "2585", 0xD0,0xC4   ;18F2585   9.0-12.5   VDD
        dt      0x0C,0xA0, "2610", 0xD1,0x00   ;18F2610   9.0-12.5   VDD
        dt      0x0C,0x80, "2620", 0xD1,0x04   ;18F2620   9.0-12.5   VDD
        dt      0x0E,0xC0, "2680", 0xD1,0x04   ;18F2680   9.0-12.5   VDD
        dt      0x21,0x40, "4221", 0xC2,0x41   ;18F4221   9.0-12.5   VDD (e)
        dt      0x21,0x00, "4321", 0xC2,0x41   ;18F4321   9.0-12.5   VDD (e)
        dt      0x10,0xE0, "4410", 0xC8,0x40   ;18F4410   9.0-12.5   VDD (e)
        dt      0x10,0xC0, "4420", 0xC8,0x41   ;18F4420   9.0-12.5   VDD (e)
        dt      0x24,0x00, "4450", 0xC8,0x40   ;18F4450   9.0-12.5   VDD (f)
check
        dt      0x0B,0x80, "4455", 0xC8,0x61   ;18F4455   9.0-12.5   VDD
        dt      0x1A,0xA0, "4480", 0xC8,0x41   ;18F4480   9.0-12.5   VDD (e)
        dt      0x10,0xA0, "4510", 0xC8,0x80   ;18F4510   9.0-12.5   VDD (e)
        dt      0x0C,0x60, "4515", 0xD0,0xC0   ;18F4515   9.0-12.5   VDD
        dt      0x10,0x80, "4520", 0xC8,0x81   ;18F4520   9.0-12.5   VDD (e)
        dt      0x0C,0x40, "4525", 0xD0,0xC4   ;18F4525   9.0-12.5   VDD
        dt      0x0B,0x40, "4550", 0xC8,0x81   ;18F4550   9.0-12.5   VDD
        dt      0x1A,0x80, "4580", 0xC8,0x81   ;18F4580   9.0-12.5   VDD (e)
        dt      0x0E,0xA0, "4585", 0xD0,0xC4   ;18F4585   9.0-12.5   VDD
        dt      0x0C,0x20, "4610", 0xD1,0x00   ;18F4610   9.0-12.5   VDD
        dt      0x0C,0x00, "4620", 0xD1,0x04   ;18F4620   9.0-12.5   VDD
        dt      0x0E,0x80, "4680", 0xD1,0x04   ;18F4680   9.0-12.5   VDD
ID8TOT  equ  ($-ID8TBL)/8


;****************************************************************
;
; 12F/16F Device Table
;
```

```
;   <ID2> <ID1> <"name"> <param1> <param2>, 8 bytes per device
;
; PARAM1 = not defined yet
;
; PARAM2 = not defined yet
;


        org     h'0E00'


ID6TBL  dt    0x00,0x00, "508 ", 0x0000;12F508
;       dt      0x00,0x00, "509 ", 0x0000      ;12F509
;       dt      0x00,0x00, "510 ", 0x0000      ;12F510
        dt      0x0F,0x80, "629 ", 0x0000      ;12F629 (*) 8.5-13.5 VPP
        dt      0x0F,0xA0, "635 ", 0x0000      ;12F635    10.0-13.0 VPP
        dt      0x0F,0xC0, "675 ", 0x0000      ;12F675 (*) 8.5-13.5 VPP
        dt      0x04,0x60, "683 ", 0x0000      ;12F683    10.0-13.0 VPP
;
;       dt      0x00,0x00, "505 ", 0x0000      ;16F505
;       dt      0x00,0x00, "506 ", 0x0000      ;16F506 future?
;       dt      0x00,0x00, "54  ", 0x0000      ;16F54  ID 12.5-13.5 VDD
;       dt      0x00,0x00, "57  ", 0x0000      ;16F57  ID 12.5-13.5 VDD
;       dt      0x00,0x00, "59  ", 0x0000      ;16F59  ID 12.5-13.5 VDD
        dt      0x07,0xA0, "627 ", 0x0000      ;16F627     8.5-13.5 VDD
        dt      0x10,0x40, "627A", 0x0000      ;16F627A   10.0-13.5 VPP
        dt      0x07,0xC0, "628 ", 0x0000      ;16F628     8.5-13.5 VDD
        dt      0x10,0x60, "628A", 0x0000      ;16F628A   10.0-13.5 VPP
        dt      0x10,0xC0, "630 ", 0x0000      ;16F630     8.5-13.5 VPP
        dt      0x10,0xA0, "636 ", 0x0000      ;16F636    10.0-13.0 VPP
;       dt      0x10,0xA0, "639 ", 0x0000      ;16F639    10.0-13.0 VPP
        dt      0x11,0x00, "648A", 0x0000      ;16F648A   10.0-13.5 VPP
        dt      0x10,0xE0, "676 ", 0x0000      ;16F676     8.5-13.5 VPP
        dt      0x10,0x80, "684 ", 0x0000      ;16F684    10.0-13.0 VPP
;       dt      0x04,0xA0, "685 ", 0x0000      ;16F685    10.0-13.0 VPP
;       dt      0x13,0x20, "687 ", 0x0000      ;16F687    10.0-13.0 VPP
        dt      0x11,0x80, "688 ", 0x0000      ;16F688    10.0-13.0 VPP
;       dt      0x13,0x40, "689 ", 0x0000      ;16F689    10.0-13.0 VPP
;       dt      0x14,0x00, "690 ", 0x0000      ;16F690    10.0-13.0 VPP
;       dt      0x11,0x40, "716 ", 0x0000      ;16F716    11.0-13.5 VDD
;       dt      0x00,0x00, "72  ", 0x0000      ;16F72


;       dt      0x06,0x00, "73  ", 0x0000      ;16F73     12.8-13.3 VDD
```

```
        dt      0x0B,0xA0, "737 ", 0x0000        ;16F737    12.8-13.3 VDD
;       dt      0x06,0x20, "74  ", 0x0000        ;16F74     12.8-13.3 VDD
        dt      0x0B,0xE0, "747 ", 0x0000        ;16F747    12.8-13.3 VDD
;       dt      0x06,0x40, "76  ", 0x0000        ;16F76     12.8-13.3 VDD
        dt      0x0E,0xA0, "767 ", 0x0000        ;16F767    12.8-13.3 VDD
;       dt      0x06,0x60, "77  ", 0x0000        ;16F77     12.8-13.3 VDD
        dt      0x0D,0xE0, "777 ", 0x0000        ;16F777    12.8-13.3 VDD


;       dt      0x12,0x00, "785 ", 0x0000        ;16F785    10.0-12.0 VDD/VPP
        dt      0x04,0xC0, "818 ", 0x0000        ;16F818     8.5-13.5 VDD
        dt      0x04,0xE0, "819 ", 0x0000        ;16F819     8.5-13.5 VDD
        dt      0x05,0x60, "84A ", 0x0000        ;16F84A
        dt      0x07,0x20, "87  ", 0x0000        ;16F87      8.5-13.5 VDD
        dt      0x0D,0x00, "870 ", 0x0000        ;16F870     8.5-13.5 VDD
        dt      0x0D,0x20, "871 ", 0x0000        ;16F871     8.5-13.5 VDD
        dt      0x08,0xE0, "872 ", 0x0000        ;16F872     8.5-13.5 VDD
        dt      0x09,0x60, "873 ", 0x0000        ;16F873     8.5-13.5 VDD
        dt      0x0E,0x40, "873A", 0x0000        ;16F873A    8.5-13.5 VDD
        dt      0x09,0x20, "874 ", 0x0000        ;16F874     8.5-13.5 VDD
        dt      0x0E,0x60, "874A", 0x0000        ;16F874A    8.5-13.5 VDD
        dt      0x09,0xE0, "876 ", 0x0000        ;16F876     8.5-13.5 VDD
        dt      0x0E,0x00, "876A", 0x0000        ;16F876A    8.5-13.5 VDD
        dt      0x09,0xA0, "877 ", 0x0000        ;16F877     8.5-13.5 VDD
        dt      0x0E,0x20, "877A", 0x0000        ;16F877A    8.5-13.5 VDD
        dt      0x07,0x60, "88  ", 0x0000        ;16F88      8.5-13.5 VDD
;       dt      0x13,0xE0, "913 ", 0x0000        ;16F913    10.0-12.0 VDD/VPP
;       dt      0x13,0xC0, "914 ", 0x0000        ;16F914    10.0-12.0 VDD/VPP
;       dt      0x13,0xA0, "916 ", 0x0000        ;16F916    10.0-12.0 VDD/VPP
;       dt      0x13,0x80, "917 ", 0x0000        ;16F917    10.0-12.0 VDD/VPP
```