Application Notes
for the
T6963C
LCD Graphics Controller Chip

October, 95

1. Introduction

The T6963C graphics controller chip is designed to control small to medium size graphic Liquid Crystal Display modules (LCD). It may be interfaced with a number of different 8-bit micro-processor units (MPU) such as the Z-80. It provides the necessary interface between the MPU and the video RAM (VRAM). It also generates the necessary timing and data signals for the liquid crystal driver circuits. It has a 128 character Character-Generator ROM (CG-ROM) and has the capability to control upto 64K bytes of external display RAM (VRAM). This VRAM may be allocated for text, graphics and external character-generator RAM (i.e. a user definable character generator). The T6963C can support a wide variety of LCD formats and has the ability to combine text and graphics data on to the LCD. A number of character attribute functions are also available.

This application note is not written with any specific display in mind but is intended to give a thorough understanding of how to use the T6963C and implement the software/hardware interface. Some LCD modules will have the T6963C controller built into the module and many of the T6963C hardware selectable features will be hardwired by the PCB traces and not user-selectable.

2. Main Functions and Features of T6963C

- Simple 8-bit parallel interface
- Hardware Selectable Display Formats: Columns: 32, 40, 64, 80
  Lines: 2, 4, 6, ... 28, 32
- Hardware Selectable Fonts(W) x (H): 5x8, 6x8, 7x8, or 8x8
- Programmable Duty Cycles: 1/16 to 1/128
- Internal 128 character CG-ROM
- Software allocation of Text, Graphic and Character Generator RAM (CG-RAM)
- Ability to mix and merge text with graphics
- Low power CMOS design
- Operates up to 5 MHz

Note: Not all these features are implemented on Densitron LCD modules with on-board T6963C controller. Check individual data sheets for details.

3. Electrical Specifications for T6963C

3.1 Absolute Maximum Ratings

(V_{SS}=0V,T_a=25 °C)

Item	Symbol	Value	Units
Power supply voltage	V_{DD}	-0.3 to +7.0	V
Input voltage	V_{in}	-0.3 to VDD+0.3	V
Operating Temperature	T_{op}	-10 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C

Note: Specification is for T6963C only. LCD module specifications may differ.

3.2 Electrical Characteristics

(V_{DD}=+5V±5%, GND=0V, T_a=+25°C)

Item		Symbol	Condition	Min	Max	Units	Notes
Operating Volatge		V_{DD}		4.5	5.5	V	
Input voltage	"H"	V_{IH}		V_{DD}-2.2	V_{DD}	V	1, 3
	"L"	V_{IL}		0	0.8	V	1, 2, 3
Output voltage	"H"	V_{OH}		V_{DD}-0.3	V_{DD}	V	3
	"L"	V_{OL}		0	0.3	V	3
Output Resistance	"H"	R_{OH}	V_{OUT}=V_{DD}-0.5	-	400	Ω	3
	"L"	R_{OL}	V_{OUT}=0.5	-	400	Ω	3
Current Consumption	Oper.	I_{DD}(1)	V_{DD}=5.0V fosc=3.0 MHz	-	6	mA	
	Halt	I_{DD}(2)		-	3	µA	
Input leakage current		I_{IL}	V_{in}=0~V_{DD}	-5	5	µA	3
Output leakage current		I_{OL}	V_{out}=0~V_{DD}	-10	10	µA	3
Internal Oscillation		fosc		0.4	5.5	MHz	
External clock frequency		fcp		-	2750	KHz	
Ext. clock rise/fall time		trcp,tfcp		-	30	ns	

Notes:

1. $\overline{CE}$, C/$\overline{D}$, $\overline{RD}$, $\overline{WR}$
2. $\overline{RES}$
3. DB0 to DB7

4. Interface Pin Connections

4.1 MPU Interface Pin Functions

Pin-outs differ for individual LCD modules with on-board controllers. Please refer to individual module data sheets for pin assignment information.

Pin Name	I/O	Pin Function
V_{SS}	-	Ground (0V)
V_{DD}	-	Logic Supply (+5V)
C/$\overline{D}$	I	Register Select: "1" = Command Register, "0" = Data Register
$\overline{RD}$	I	Read Select (Active Low) - MPU ⇐ T6963C
$\overline{WR}$	I	Write Select (Active Low) - MPU ⇒ T6963C
$\overline{CE}$	I	Chip Enable (Active Low)
DB0	I/O	Bi-directional Data Bus Line 0
DB1	I/O	Bi-directional Data Bus Line 1
DB2	I/O	Bi-directional Data Bus Line 2
DB3	I/O	Bi-directional Data Bus Line 3
DB4	I/O	Bi-directional Data Bus Line 4
DB5	I/O	Bi-directional Data Bus Line 5
DB6	I/O	Bi-directional Data Bus Line 6
DB7	I/O	Bi-directional Data Bus Line 7
$\overline{RES}$	I	Reset (Active Low)
FS1	I	Font Select 6x8 font: FS1="H" 8x8 font FS1="L"
MD2	I	Mode Select 40 columns MD2="H" 32 columns MD2="H"

Notes:

1. After power on, it is necessary to keep $\overline{RES}$ low for upto 6 clock cycles of the T6963C.
2. It is necessary to guard all signals from external noise as the signal lines are directly connected to CMOS inputs and are not pulled-up or pulled-down internally, the $\overline{RES}$ is internally pulled high.
3. Font size set be FS1 line times # of columns set by MD2 line should equal the # of horizontal pixel. (i.e. if you have a 64x240 display, using a 6x8 font, then MD2 should be high to represent 40 columns. Due to the fact that 6x40 =240)

4.2 LCD Interface Pin Functions

For LCD modules with on-board controllers, these signals are not generally accessible; they are accessable on the SGI-01 serial interface card with the on-board T6963C option installed; refer to individual LCD module data sheets for pin assignments.

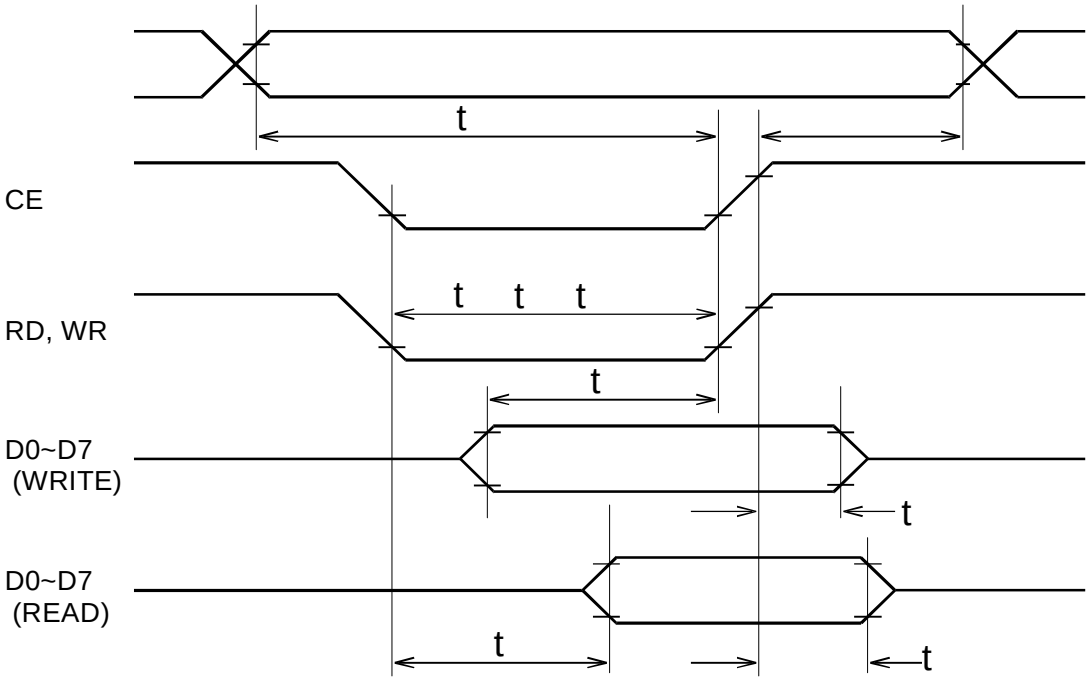
Pin Name	I/O	Pin Function
D1	O	Serial Data Line 1
FLM (CDATA)	O	First Line Marker (Start of Frame)
M (FR)	O	Control Signal for AC drive of LC
CL1 (LP)	O	Latch clock
CL2 (SCP)	O	Shift clock for serial data
D2	O	Serial Data Line 2
V_{DD}	-	Power supply for logic circuits
V_{SS}	-	Ground
V_{EE}	-	Power supply for LC drivers

V_O	-	Operating voltage for LC drivers (Contrast)

5. Timing Characteristics

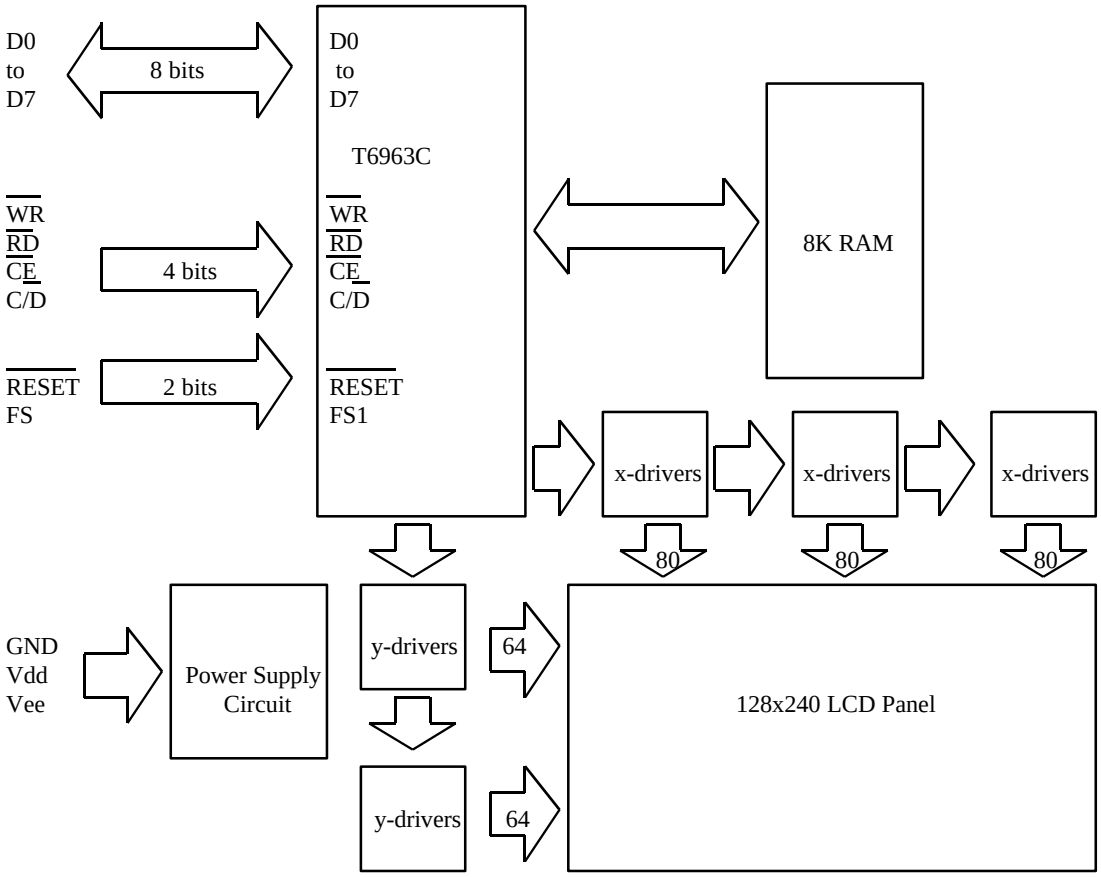
MPU Interface Timing (MPU ⇔ T6963C)

Item	Symbol	Min	Typ	Max	Unit
C/$\overline{D}$ Set Up Time	t_{CDS}	100	-	-	ns
C/$\overline{D}$ Hold Time	t_{CDH}	10	-	-	ns
$\overline{CE}$, $\overline{RD}$, $\overline{WR}$ Pulse Width	t_{CE}, t_{RD}, t_{WR}	80	-	-	ns
Data Set Up Time	t_{DS}	80	-	-	ns
Data Hold Time	t_{DH}	40	-	-	ns
Access time	t_{ACC}	-	-	150	ns
Output Hold Time	t_{OH}	10	-	50	ns



6. System Block Diagram

All liquid crystal displays require two power sources, V_{DD} for logic circuits and V_{EE} for Liquid Crystal (LC) drive. Some graphics LCD modules will run directly of a single V_{DD} supply by generating the V_{EE} voltage on-board; others will require an external DC-DC converter to generate the negative V_{EE} voltage. Refer to individual specifications for details.

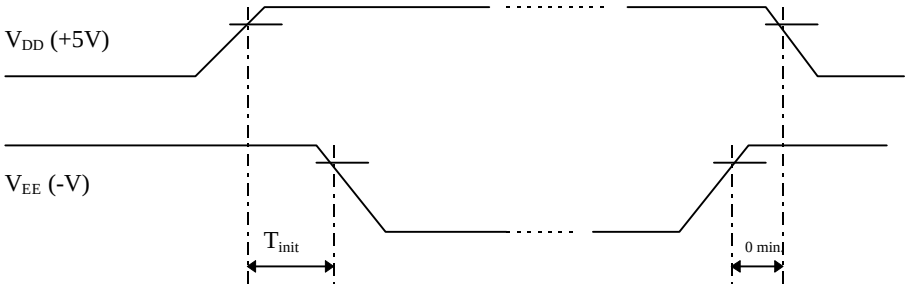


7. Power Supply Considerations and /RES Terminal

7.1 Power Supply Sequencing

To prevent latch-up of the CMOS LSI (T6963C and LCD driver LSI) ensure your system power supply follows the following sequence. It is very important to follow this sequence in order to prevent the CMOS LSI from latching up and to prevent DC signals from being applied to the LC material. If the VEE voltage is applied before timing signals M, CL1, CL2, and FLM then a DC voltage signal will be applied to the LC material. Over time this will degrade the LC fluid performance due to an electro-chemical effect. If this power-up sequence is not adherred to, permanent damage to the LCD module may result.

After power on it is necessary to keep /RES terminal low for six oscillator clock cycles to ensure proper reset of the T6963C. If T6963C is reset during normal operation ensure that the V_{EE} voltage to the LCD is disabled until the T6963C registers are re-initialized.



Where T_{init} is the time taken to initialize the T6963C

Figure 7.1: Power Supply Sequence

7.2 The /RES (RESET) Terminal

The T6963C may be reset by an external active low TTL signal from a MPU or other logic device or it may be reset using the following circuit.

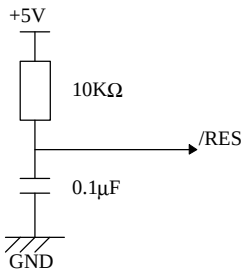


Figure 7.2: RESET Circuit

8. T6963C Instruction Set

Table 8.0: T6963C Instruction Set

Commands	D7	D6	D5	D4	D3	D2	D1	D0	Description	Execute Time
Pointer Set	**0**	**0**	**1**	**0**	**0**	**N2**	**N1**	**N0**		**Status check**
						0	0	1	**Cursor Pointer Set**	
						0	1	0	**Offset Register Set**	
						1	0	0	**Address Pointer Set**	
Control Word Set Commands	**0**	**1**	**0**	**0**	**0**	**0**	**N1**	**N0**		**32 x 1/fosc**
							0	0	**Text Home Address Set**	
							0	1	**Text Area Set**	
							1	0	**Graphic Home Address Set**	
							1	1	**Graphic Area Set**	
Mode Set	**1**	**0**	**0**	**0**	**CG**	**N2**	**N1**	**N0**		**32 x 1/fosc**
					0				**CG ROM Mode**	
					1				**CG RAM Mode**	

2. Read the status of the STA0 and STA1 Flags before each new command or data byte is sent to the T6963C. If these two flags are set (i.e.=1) then the T6963C is not busy processing the previous instruction and it is safe to write a new command or data byte to the T6963C. If a new instruction is sent to the T6963C while these two flags are not set (i.e.=0), then that command shall be ignored by the T6963C.
3. In the case of a dual screen LCD the screen copy command should not be used.

8.1 Description of Pointer Set Commands (Two data bytes plus Command byte)

8.1.1 Cursor Pointer Set

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
First argument (0-7FH)	*	Cursor Column Position (Character)						
Second argument (0-1FH)	*	*	*	Cursor Row Position (Character)				
Cursor Pointer Set (21H)	0	0	1	0	0	0	0	1

The cursor Pointer Set command has two data bytes associated with it to specify the character position for the cursor. This is the only command which will shift or move the cursor. The cursor is not shifted by Data write commands. Cursor position should be set to be within actual display area.

8.1.2 Offset Register Set

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
First argument (0-1FH)	*	*	*	CG-RAM Address				
Second argument (00H)	0	0	0	0	0	0	0	0
Offset Register Set (22H)	0	0	1	0	0	0	1	0

The lower five bits of the first data byte should be set to the upper 5 bits of the start address for the character generator RAM (CG-RAM) area. The second data byte should be set to zero. Refer to section 11.0 for details regarding the use of the CG-RAM area.

8.1.3 Address Pointer Set

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
First argument (0-FFH)	Address Pointer (lower)							
Second argument (0-FFH)	Address Pointer (upper)							
Address Pointer Set (24H)	0	0	1	0	0	1	0	0

The Address Pointer Set command is used to specify the start address for writing data to the video RAM (VRAM) or for reading data from the VRAM. The address should be set to a location in the actual display RAM area specified by the memory map for a given module. Refer to individual module specifications for details.

8.2 Description of Control Word Set Commands (Two data bytes plus Command byte)

8.2.1 Text Home Address Set (TH)

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
First argument (0-FFH)	Text Home Address (TH lower)							
Second argument (0-FFH)	Text Home Address (TH upper)							
Text Home Address Set (40H)	0	1	0	0	0	0	0	0

This command defines the starting address of VRAM for text display data. The data stored in the Text Home (TH) Address will be displayed at the top left hand character position (the home position).

8.2.2 Text Area Set (TA)

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
First argument (0-FFH)	Number of columns of characters (TA)							
Second argument (00H)	00H							
Text Area Set (41H)	0	1	0	0	0	0	0	1

This command defines the number of columns of text for the Text area of VRAM. The Text Area (TA) may be set independantly of the number of characters per line set by hardware settings on the T6963C controller chip. It is usual to set the TA to the same number of characters per line as the

Text only (with Attribute data in Graphic Area)	1	0	0	0	*	1	0	0

8.4 Description of Display Mode Set Commands (Command byte only)

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Display Off (90H)	1	0	0	1	0	0	0	0
Cursor On, Blink Off	1	0	0	1	*	*	1	0
Cursor On, Blink On	1	0	0	1	*	*	1	1
Text On, Graphic Off	1	0	0	1	0	1	*	*
Text Off, Graphic On	1	0	0	1	1	0	*	*
Text On, Graphic On	1	0	0	1	1	1	*	*

Cursor Blink : Enabled - Set D0 (N0=1)
Disabled - Reset D0 (N0=0)

Cursor Enable: Enabled - Set D1 (N1=1)
Disabled -Reset D1 (N1=0)

Text Enable : Enabled - Set D2 (N2=1)
Disabled - Reset D2 (N2=0)

Graphic Enable: Enabled - Set D3 (N1=3)
Disabled -Reset D3 (N1=3)

After Reset N3-N0 are reset to zero.

8.5 Description of Cursor Pattern Select Command (Command byte only)

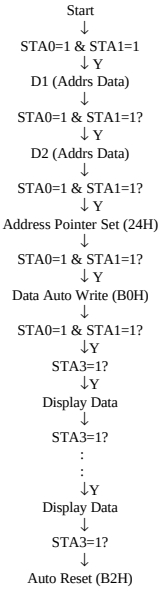
Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1 line cursor (A0H)	1	0	1	0	0	0	0	0
2 line cursor (A1H)	1	0	1	0	0	0	0	1
"	"	"	"	"	"	"	"	"
"	"	"	"	"	"	"	"	"
7 line cursor (A6H)	1	0	1	0	0	1	1	0
8 line cursor (A7H)	1	0	1	0	0	1	1	1

This single byte command selects the type of cursor displayed when the cursor is enabled. For a single underline type cursor send command “A0H”. If a block style cursor is required sent command “A7H”.

8.6 Description of Data Auto Read/Write Commands (Command byte only)

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data Auto Write Set (B0H)	1	0	1	1	0	0	0	0
Data Auto Read Set (B1H)	1	0	1	1	0	0	0	1
Auto Mode Reset (B2H or B3H)	1	0	1	1	0	0	1	*

These single byte commands are useful when transferring blocks of data to or from the VRAM. After sending a Data Auto Write (B0H)or Data Auto Read (B1H) command it is not necessary to send Data Write or Data Read instructions (section 8.7) for each data byte being written to or read from the VRAM. Data Auto Write and Data Auto Read commands should follow the Address Pointer Set command (section 8.1.3). The Address Pointer will automatically increment by 1 for each data written or data read. After sending (or receiving) all data the Auto Mode Reset command (B2H or B3H) should be sent to return to normal operation. Note that no commands can be accepted when in Data Auto Write or Data Auto Read modes, as all bytes written or read are assumed to be display data bytes.



8.7 Description of Data Read/Data Write Commands (Command byte only)

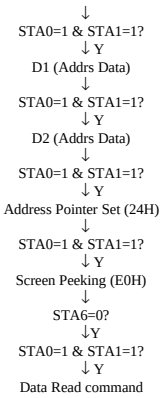
Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Data Write - Address Pointer Auto Incremented (C0H)	1	1	0	0	0	0	0	0
Data Read - Address Pointer Auto Incremented (C1H)	1	1	0	0	0	0	0	1
Data Write - Address Pointer Auto Decremented (C2H)	1	1	0	0	0	0	1	0
Data Read - Address Pointer Auto Decremented (C3H)	1	1	0	0	0	0	1	1
Data Write - Address Pointer Auto Unchanged (C4H)	1	1	0	0	0	1	*	0
Data Read - Address Pointer Auto Unchanged (C5H)	1	1	0	0	0	1	*	1

These commands are used to write data to or read data from the VRAM. Data Read or Data Write commands should be sent after setting an address by the Pointer Set command (section 8.1.3). The Address Pointr may be automatically incremented , decremented or left unchanged depending on which Data Read/Write command is being sent. A Data Write or Data Read command is required for each data byte written to or read from the VRAM.

8.8 Description of Screen Peeking Command (Command byte only)

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Screen Peeking (E0H)	1	1	1	0	0	0	0	0

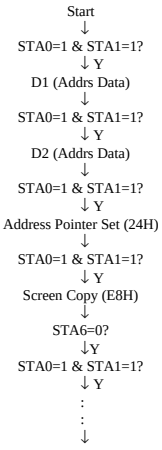
This single byte command is used to transfer 1 byte of displayed data to the data stack and may be read by the MPU using a Data Read command (section 8.7). This command is useful to read the logical combination of text and graphic data on the LCD screen. The Status flag STA6 should be checked after each Screen Peeking (E0H)command. If the Address Pointer (section 8.1.3) is not set to the Graphic RAM area, then the Screen Peeking command is ignored and STA6 is set to "1".



8.9 Description of Screen Copy Command (Command byte only)

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Screen Copy (E8H)	1	1	1	0	1	0	0	0

This single byte command is used to copy 1 row of data displayed on the LCD screen to the Graphic RAM area specified by the Address Pointer Set command (section 8.1.3). This Screen Copy command (E8H) cannot be used if the row of displayed data contains Text Attribute data as set by the Mode Set command (section 8.3). The Status flag STA6 should be checked after each Screen Copy command. If the Address Pointer (section 8.1.3) is not set to the Graphic RAM area, then the Screen Copy command is ignored and STA6 is set to "1".



8.10 Description of Bit Set/Bit Reset Command (Command byte only)

Description (Range)	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit Reset (F0H-F7H)	1	1	1	1	0	N2	N1	N0
Bit Set (F8H-FFH)	1	1	1	1	1	N2	N1	N0

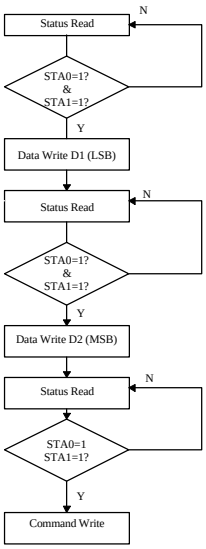
This single byte command is used to set/reset individual bits in the RAM. This command allows one bit in the byte pointed to by the Address Pointer Set command (section 8.1.3) to be set or reset. Multiple bits in a byte cannot be set/reset at the same time. N0~N2 specifies the location of the bit to set/reset. 000 selects the least significant bit (LSB) and 111 the most significant bit (MSB).

9. Communication between MPU and T6963C

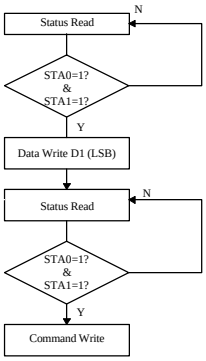
The T6963C communicates asynchronously with the MPU clock. The following procedures are required for data transmission between the T6963C and the MPU.

9.1 Data Transmission Methods

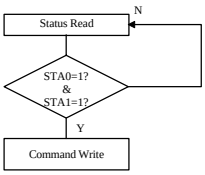
9.1.1 Commands with 2 data bytes



9.1.2 Commands with 1data byte



9.1.3 Commands with no data



9.1.4 Data Auto Write & Data Auto Read Commands

With either the Data Auto Read or Data Auto Write commands ensure that STA2 and STA3 of the Status Read register are checked between all data and command Read/Writes to verify that the T6963C for Data Read(STA2) or Data Write (STA3). (Refer to section 8.6)

9.1.5 Screen Peeking and Screen Copy Commands

With either the Screen Peeking and Screen Copy commands ensure that STA6 of the Status Read register is checked, to verify that the Address Pointer is set to within the Graphic RAM area. (Refer to section 8.8 and 8.9)

9.2 Status Read

The Status of the T6963C should be checked before all command and data bytes are sent to/from the T6963C. The Status register may be read from the 8-bit data lines (DB0~DB7), by setting C/D = "H", /WR="H", /CE="L" and /RD="L".

Description	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0
Status Read Reg.	BLINK	ERROR	CLR	-	DAWRDY	DARRDY	BUSY2	BUSY1
	MSB							LSB

Note:
1. It is necessary to read STA0 and STA1 at the same time before an instruction is executed.
2. STA2 and STA3 are only valid during Data Auto Read/Write modes. In the Data Auto Read/Write modes STA0 and STA1 are invalid
3. If data is tranferred while either STA0 or STA1 = "0" then that data is ignored by T6963C.

Status Bit	Description	Function
STA0 (BUSY1)	Busy flag to indicate whether T6963C is ready to accept instruction	"0" =NOT READY "1" =READY
STA1 (BUSY2)	Busy flag to indicate whether T693C is ready to accept data read or write	"0" =NOT READY "1" =READY
STA2 (DARRDY)	Data Auto Read Ready flag (Only valid in Data Auto Read/Write modes (section 8.6))	"0" =NOT READY "1" =READY
STA3 (DAWRDY)	Data Auto Read Ready flag (Only valid in Data Auto Read/Write modes (section 8.6))	"0" =NOT READY "1" =READY
STA4	-	- -
STA5 (CLR)	Clear flag indicating operation of the T6963C	"0" =NOT CLEARED "1" =CLEARED & Operating
STA6 (ERROR)	Error flag for Screen Peeking and Screen Copy commands (section 8.8 & 8.9)	"0" =Address Pointer Valid "1" =Address Pointer out of Graphic Area
STA7 (BLINK)	Blink flag to indicate status of Blink condition	"0" =Display OFF "1" =Normal (Display ON)

10. Memory Addressing and Display Position

This section describes the relationship between the T6963C display memory (VRAM) and the display position on the LCD screen. Text Home address (TH); Text Area number (TA); Graphic Home address (GH) and Graphic Area number (GA) are also described in this section. TH, TA, GH and GA are set by the Control Word Set command described in sections 8.2.1 - 8.2.4. TH defines the starting address for Text data in the VRAM, GH defines the starting address for Graphic data in the VRAM for graphics modes and the starting address for Text Attribute data in Attribute mode (Refer to section 11.3). TA defines the number of columns of text on a LCD screen and GA sets the number of display bytes per line on a LCD screen.

10.1 The case of single screen drive LCD's

The relationship between display memory addresses and display position on a single drive LCD screen is shown below for both Text and Graphic Areas.

10.1.1 Text Display Area for single screen LCD's

TH	TH+1	--------	TH+CL-1	TH+CL	↑
TH+TA	TH+TA+1	:	TH+TA+CL-1	TH+TA+CL	|
:	:	:	:	:	m lines
:	:	:	:	:	of text
TH+(m-2)TA	TH+(m-2)TA+1	--------	TH+(m-1)TA+CL-1	TH+(m-1)TA+CL	|
TH+(m-1)TA	TH+(m-1)TA+1	--------	TH+mTA+CL-1	TH+mTA+CL	↓

←——————————X characters per line——————————→

10.1.2 Graphic Display Area for single screen LCD's

GH	GH+1	--------	GH+CL-1	GH+CL	↑
GH+GA	GH+GA+1	:	GH+GA+CL-1	GH+GA+CL	|
:	:	:	:	:	n rows
:	:	:	:	:	of dots
GH+(n-2)GA	GH+(n-2)GA+1	--------	GH+(n-1)GA+CL-1	GH+(n-1)GA+CL	|
GH+(n-1)GA	GH+(n-1)GA+1	--------	GH+nGA+CL-1	GH+nGA+CL	↓

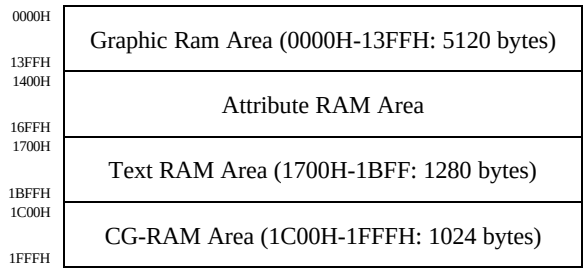
←——————————Y dots per line——————————→

Where:

Display Format	Font Size	Text Display			Graphics Display			CL+1 typ.
		X	m	TA	Y	n	GA	
64x120	6x8	20	8	14H	120	64	14H	14H
1/64 duty	8x8	15	8	0FH	120	64	0FH	0FH
128x128	6x8	21	16	16H	128	128	16H	16H
1/128 duty	8x8	16	16	10H	128	128	10H	10H
64x240	6x8	40	8	28H	240	64	28H	28H
1/64 duty	8x8	30	8	1EH	240	64	1EH	1EH
128x240	6x8	40	16	28H	240	128	28H	28H
1/128 duty	8x8	30	16	1EH	240	128	1EH	1EH

Note: In the case of the Graphics Area with 6x8 font size selected, the most significant bits D6 and D7 of graphics data are ignored, and not displayed on the LCD screen.

10.1.3 Example RAM Map for single screen drive LCD



Note: This example shows RAM map for "CG-ROM" mode (section 8.3 & 11). If "CG-RAM" mode is required allocat 2048 bytes for CG-RAM area

The Display RAM (VRAM) is usually built onto the LCD module along with T6963C and LCD driver LSI chips. The T6963C automatically reads data from the VRAM, processes it and sendsit out to the LCD LSI driver chips. The Control Word Set commands (section 8.2) are used to set the Text Home, Graphic Home and Text/Graphics Areas. The VRAM map made be changed to suit the users preference. The above RAM map is just an example. If more than one screen can be stored in the RAM, vertical scrolling and paging can be performed, by resetting the Text Home and Graphic Home addresses. Usually LCD modules with on-board T6963C controllers have 4K or 8K byes of RAM, check individual LCD module specifications for RAM size information.

10.2 The case of dual screen drive LCD's

The relationship between display memory addresses and display position on a dual drive LCD screen is shown below for both Text and Graphic Areas.

10.2.1 Text Display Area for dual screen LCD's

TH	TH+1	-----	TH+CL-1	TH+CL	↑
TH+TA	TH+TA+1	:	TH+TA+CL-1	TH+TA+CL	|
:	:	:	:	:	m lines
:	:	:	:	:	of text
TH+(m-1)TA	TH+(m-1)TA+1	-----	TH+mTA+CL-1	TH+mTA+CL	↓
TH+8000H	TH+8000H+1	-----	TH+8000H+TA+CL-1	TH+8000H+TA+CL	↑
:	:	:	:	:	|
:	:	:	:	:	m lines
TH+8000H+(m-2)TA	TH+8000H+(m-2)TA+1	-----	TH+8000H+(m-1)TA+CL-1	TH+8000H+(m-1)TA+CL	of text
TH+8000H+(m-1)TA	TH+8000H+(m-1)TA+1	-----	TH+8000H+mTA+CL-1	TH+8000H+mTA+CL	↓

←————————————————X characters per line————————————————→

10.2.2 Graphic Display Area for dual screen LCD's

GH	GH+1	----	GH+CL-1	GH+CL	↑
GH+GA	GH+GA+1	:	GH+GA+CL-1	GH+GA+CL	|
:	:	:	:	:	n rows
:	:	:	:	:	of dots
GH+(m-1)GA	GH+(m-1)GA+1	----	GH+mGA+CL-1	GH+mGA+CL	↓
GH+8000H	GH+8000H+1	----	GH+8000H+GA+CL-1	GH+8000H+GA+CL	↑
:	:	:	:	:	|
:	:	:	:	:	n rows
GH+8000H+(m-2)GA	GH+8000H+(m-2)GA+1	----	GH+8000H+(m-1)GA+CL-1	GH+8000H+(m-1)GA+CL	of dots
GH+8000H+(m-1)GA	GH+8000H+(m-1)GA+1	----	GH+8000H+mGA+CL-1	GH+8000H+mGA+CL	↓

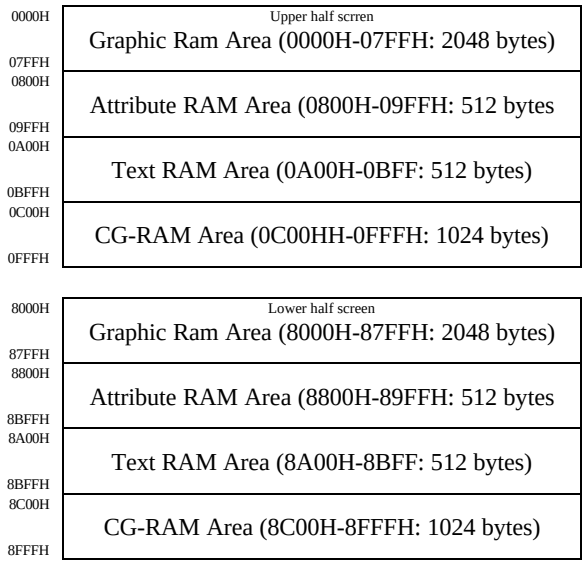
←————————————————————Y dots per line————————————————————→

Where:

Display Format	Font Size	Text Display			Graphics Display			CL+1 typ.
		X	m	TA	Y	n	GA	
64x120	6x8	20	4	14H	120	32	14H	14H
1/32 duty	8x8	15	4	0FH	120	32	0FH	0FH
128x160	6x8	21	8	16H	128	64	16H	16H
1/64 duty	8x8	16	8	10H	128	64	10H	10H
64x240	6x8	40	4	28H	240	32	28H	28H
1/32 duty	8x8	30	4	1EH	240	32	1EH	1EH
128x256	6x8	40	8	2BH	256	64	2BH	2BH
1/64 duty	8x8	30	8	20H	256	64	20H	20H

Note: In the case of the Graphics Area with 6x8 font size selected, the most significant bits D6 and D7 of graphics data are ignored, and not displayed on the LCD screen.

10.2.3 Example RAM Map for dual screen drive LCD



Note: This example shows RAM map for "CG-ROM" mode (section 8.3 & 11). If "CG-RAM" mode is required allocat 2048 bytes for CG-RAM area

The above is just an example of a suitable RAM map for a dual drive LCD screen. The Control Word Set commands (section 8.2) are used to set the Text Home, Graphic Home and Text/Graphics Areas. The VRAM map made be changed to suit the users preferences.

11. T6963C Character Generator and Character Attribute Functions

There are two character generator functions built into the T6963C, namely internal CG-ROM and external CG-RAM (Using Display data RAM). When the CG bit of the Mode Set command (section 8.3) is “0” the CG-ROM and CG-RAM have 128 character capability. If the CG bit is “1” then there is no internal CG-ROM function available but 256 character capability for the external CG-RAM.

11.1 Internal Character Generator ROM (CG-ROM)

Refer to section 14 for the charater font table stored in the CG-ROM area. Note that the CG bit of the Mode Set command needs to be set to “0” to make use of the sCG-ROM feature.

11.2 User Defined Character Generator RAM (CG-RAM)

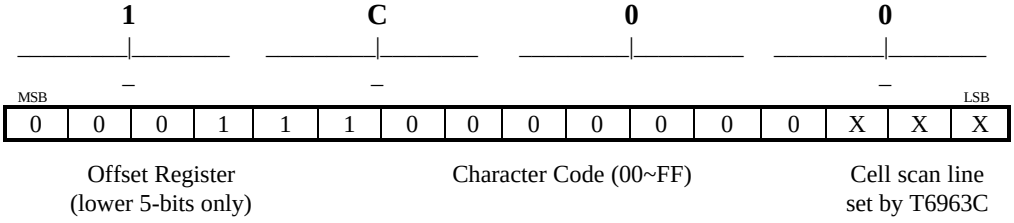
The internal CG-RAM is an area of memory where the user can program custom characters and retrieve them later by using the appropriate Character codes.

To use the external CG-RAM it is first necessary to set the Offset register (section 8.1.2) which specifies the location of RAM to be used. The user must program the CG-RAM with the desired custom character patterns. Once programmed, the external CG-RAM can then be used in place of, or inconjunction with, the internal CG-ROM.

The CG bit of the Mode Set command (section 8.3) controls the configuration of the internal CG-ROM and external CG-RAM.

When CG bit = “0”: Both CG-ROM codes in the range 00H-7FH and CG-RAM codes in the range 80H-FFH are valid. Each character in the CG-RAM area will require 8-bytes of data resulting in a memory requirement of 0400H. So if we choose to locate the CG-RAM at 1C00H we should set the Offset register to 03H as this defines the upper 5-bits of the CG-RAM address.

When CG bit = “1” Only CG-RAM codes 00H-FFH are valid. Access to CG-ROM area is not possible. Each character in the CG-RAM area will require 8-bytes of data resulting in a memory requirement of 0800H. So if we choose to locate the CG-RAM at 1800H we should set the Offset register to 03H as this defines the upper 5-bits of the CG-RAM address



For example to load up the character pattern for the pound sign “#” to character code 0FH in the CG-RAM area starting at 1C00H. The Address Pointer should be set to 1C78H by the Address Pointer Set command (section 8.1.3) and then the following eight bytes [06,06,1F,06,06,1F,06,00]should be written to the CG-RAM area using eight succesive Data Write (C0H) commands.

11.3 Character Attribute Function

The attribute function is used for setting “inverse video” (negative image) and/or “blinking” display.

To use the Attribute function , it is first necessary to reassign the Graphic Home address to the first address of the Attribute RAM area by using the internal RAM write command. Please note that Graphic data cannot be displayed while using the Attribute function. Second, it is necessary to to enter the desired Attribute data using the Data Write command (section 8.7). The following table defines the function of Attribute data.

Description	D7	D6	D5	D4	D3	D2	D1	D0
Normal Display (Text only)	*	*	*	*	0	0	0	0
Reverse Display (Text only)	*	*	*	*	0	1	0	1
Inhibit display	*	*	*	*	0	0	1	1
Blink of normal display	*	*	*	*	1	0	0	0
Blink of reverse display	*	*	*	*	1	1	0	1
inhibit display	*	*	*	*	1	0	1	1

The Attribute Data for the first character in Text RAM area should be written into the first byte of the Attribute RAM area, and the Attribute data of the nth character should be written to the nth byte in the Attribute RAM area. Therefore if the Text RAM area set by the Text Home address Set command (section 8.2.1) is 1700H and the Attribute RAM is set to 1400H by the Graphic Home address Set command (section 8.2.3) then to set the Reverse Blink attribute of the 16th character of the first line of dislayed text, the value 0DH sould be written to location 140FH by the Data Write command (section 8.7). The address 140FH may need to be set up by the Address Pointer Set command (section 8.1.3).

12. Recommended Initialization

The Mode Set and Control Word Set commands must be initialized after power is turned ON. These command define what size display the T6963C is to control and which mode to run in.

Commands	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
Power On.	Power On										
Hard Reset (/RES)	/RES="L" (1 msec min. After V_{DD}>4.75V)										
Mode Set	1	1	0	0	0	0	0	0	0	80H	"OR" , "CG-ROM" Mode
Control Word Set	0	0	0	0	0	0	0	0	0	00H	Graphic Home address data
	0	0	0	0	0	0	0	0	0	00H	GH=0000H
Graphic Home Address Set	1	0	1	0	0	0	0	1	0	42H	Graphic Home Address Set command
Control Word Set	0	*	*	*	*	*	*	*	*	*	See section 10.1.2 for value of GA data
	0	*	*	*	*	*	*	*	*	*	
Graphic Home Address Set	1	0	1	0	0	0	0	1	1	43H	Graphic Area Set command
Control Word Set	0	*	*	*	*	*	*	*	*	*	See section 10.1.2 for value of TH data
	0	*	*	*	*	*	*	*	*	*	TH=****H
Text Home Address Set	1	0	1	0	0	0	0	0	0	40H	Text Home Address Set command
Control Word Set	0	*	*	*	*	*	*	*	*	*	See section 10.1.2 for value of TA data
	0	*	*	*	*	*	*	*	*	*	TA=****H
Text Home Address Set	1	0	1	0	0	0	0	0	1	41H	Text Area Set command
Initialisation Ends----------	----------										----------
-	------										------
Address Pointer Set	0	*	*	*	*	*	*	*	*	*	Text Home address data (section 10.1.2)
	0	*	*	*	*	*	*	*	*	*	TH=****H
	1	0	0	1	0	0	1	0	0	24H	Address Pointer Set command
Data Write (Text) D	0	0	0	1	0	0	1	0	0	24H	Character code 24H="D"
	1	1	1	0	0	0	0	0	0	C0H	Data Write Autoincrement
Data Write (Text) E	0	0	0	1	0	0	1	0	1	25H	Character code 25H="E"
|	1	1	1	0	0	0	0	0	0	C0H	Data Write Autoincrement

13. Trouble shooting Guide

Symptoms	Possible Solutions
Display appears blank	1, 2, 3, 5, 6, 7, 8, 9, 10, 12, 13, 14
Displayed data enters unreliably or at random	2, 3, 4
Missing column segments or pixels	13
Excessive heat generated by LSI chips or excessive I_{DD} current	1, 14
Unable to read VRAM or Busy flag	1, 3, 7, 9, 10
EL Backlight will not function or is too dim	15
LED backlight will not function or is too bright or runs too hot	11

Possible Solutions:

1. Check voltage level and polarity of V_{DD} and V_{SS} at display connector. The V_{DD} logic supply voltage should be in the range 4.75VDC < V_{DD} < 5.25VDC with respect to V_{SS}(GND). Also check that V_{DD} and V_{SS} noise, is within limits.

2. Check the pulse width of /RES is within specified limits or the T6963C will not be reset properly and internal registers will not be initialized. Also check when testing numerous displays on the same test set-up that the V_{DD} voltage is turned off before connecting or disconnecting LCD modules. Note that on power-up the contents of the VRAM are not cleared and will contain random data. It is best to set every location of VRAM to a known state as part of any initialization procedure.

3. Check that that all Hold and Set-up timing requirements are met as shown in section 5.1.

4. Ensure that data is not being transmitted too fast to the T6963C. Always pole the BUSY flags STA0 and STA1 before sending instructions (section 9.2). If MPU is not set up to read the BUSY flag before writing instructions allow an adequate delay between instructions (section 8). .

5. Check the voltage level at the V_O pin is at the correct voltage for the ambient temperature conditions as specified by individual LCD module data sheets.

6. Check the continuity of the cable between the host MPU and the LCD module. Check for broken connections, loose crimps or dry joints on soldered connections. Minimize the length of this cable to reduce cross-talk and noise pick-up.

7. Check that the data bus of the T6963C (DB0-DB7) is not excessively loaded during read operations.

8. Check the voltage levels of input signals is as specified by the LCD module data sheet.

9. Check that no more than one external bus device is selected during read operations so as to cause bus contention and erroneous data transfer.

10. Check for damage to PCB traces and plated through Via holes.

11. Check that the correct series current limiting resistor for the LED backlight is in place between the power supply and the LED lamp. Check individual LCD module data sheets for maximum forward current, If, for LED backlight. The LED's may burn-out if the maximum forward current, If, is exceeded. Some, but not all, LED backlight modules will already have the current limiting resistor on-board.

12. Check that Display ON/OFF flag is set otherwise display will appear blank.

13. Check that LCD module has not been mishandled by applying excessive shock of mechanical stress which will cause the LC glass to misalign with the Elastomer/Zebra strips that connect the LC glass to the PCB.

14. Check that LCD module has not been mishandled by applying excessive electrical stress in the form of electro-static discharge (ESD) or by applying reverse voltage to V_{DD} and V_{SS}. Always use electro-static handling precautions, grounded wrist straps and bench mats when handling LCD modules as they use CMOS LSI chips. Always use a grounded soldering iron when mounting connectors to the LCD module.

15. Check connections between EL backlight DC-AC inverter and the EL lamp mounted on the LCD module. Check input voltage to DC-AC inverter. Never operate the DC-AC inverter without an EL Lamp load, as this may damage the inverter. EL backlights dim with age and need to be replaced when their brightness level is no longer adequate.

14.0 Internal Character Generator Font Pattern and Character Codes

The internal character generator ROM (CG-ROM) has 128 characters stored in it. The Mode Set command (section 8.3) should be set for CG-ROM mode before using this builtin CG-ROM. The character pattern for each character code is shown in the following chart. They are 5x7 characters in an 8x8 character cell.

↓MSB LSB→	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	blank	!	“	#	$	%	&	‘	(	)	*	+	,	-	.	/
1	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
2	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
3	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
4	\	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
5	p	q	r	s	t	u	v	w	x	y	z	{	:	}	~	blank
6	Ç	ü	é	â	ä	à	å	ç	ê	ë	è	ï	î	ì	Ä	Å
7	É			ô	ö	ò	û	ù	ÿ	ö	ü	¢	£	¥		*f*